



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,695	07/24/2003	Kazuhiro Nakajima	8053-1016	9942
466	7590	01/05/2005	EXAMINER	
YOUNG & THOMPSON			NADAV, ORI	
745 SOUTH 23RD STREET				
2ND FLOOR			ART UNIT	PAPER NUMBER
ARLINGTON, VA 22202				2811

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.	10/625,695	Applicant(s)	NAKAJIMA ET AL.
Examiner	ori nadav	Art Unit	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

### A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) Responsive to communication(s) filed on 19 October 2004.  
2a) This action is FINAL.                    2b) This action is non-final.  
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) Claim(s) \_\_\_\_\_ is/are allowed.  
6) Claim(s) 1-8 is/are rejected.  
7) Claim(s) \_\_\_\_\_ is/are objected to.  
8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) The specification is objected to by the Examiner.  
10) The drawing(s) filed on 24 July 2003 is/are: a) accepted or b) objected to by the Examiner.  
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:  
    1. Certified copies of the priority documents have been received.  
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
    Paper No(s)/Mail Date 7/24/03.
- 4) Interview Summary (PTO-413)  
    Paper No(s)/Mail Date. \_\_\_\_\_.  
5) Notice of Informal Patent Application (PTO-152)  
6) Other: \_\_\_\_\_.

**DETAILED ACTION**

***Election/Restrictions***

Applicant's election without traverse of claims 1-8 in the reply filed on 10/19/2004 is acknowledged.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant Admitted Prior Art (AAPA).

AAPA teaches in figures 16 and 17 and related text (pages 1-5 and 35-38) a production process for producing plurality of a semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first wiring-arrangement section on each of said chip areas;

subjecting said wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device by forming a second wiring-arrangement section on said first wiring-arrangement section when said wafer passes said provisional yield-rate test,

wherein a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said provision yield-rate test when said yield-rate exceeds a predetermined permissible rate,

wherein said first wiring-arrangement section is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and said second wiring-arrangement section is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request,

wherein said basic wiring-arrangement section has a plurality of electrode pads 58' formed an uppermost surface thereof, for carrying out said provisional yield-rate test,

subjecting said wafer to a genuine yield-rate test which it is examined whether each of the finished semiconductor devices on said wafer is acceptable or unacceptable thereby find a yield-rate of acceptable finished semiconductor devices; and finally processing said wafer when said wafer passes said genuine yield-rate test,

Art Unit: 2811

wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate, wherein said customized wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface thereof, and said genuine yield-rate test is carried out, using the electrode pads of said customized wiring-arrangement section,

wherein said basic wiring-arrangement section is formed as a multi-layered wiring-arrangement section 16' (see figure 16) composed at least two metal circuit pattern layers 36', 40' and at least one insulation layer 38' alternately laminated on each of said chip areas, and said customized wiring-arrangement section 48' is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer 54 alternately laminated on said basic wiring-arrangement section.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A-C are cited as being related to a production process.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC**

**2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.  
1/4/05

ORI NADAV  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800